

Fig.2

FIFO STATUS	DATA PRESENCE		DATA ABSENCE	
	FIRST BIT	SECOND BIT	FIRST BIT	SECOND BIT
DATA	1(0)	1(0)	×	×
DATA TIMING	0	1	0	0

Fig.3

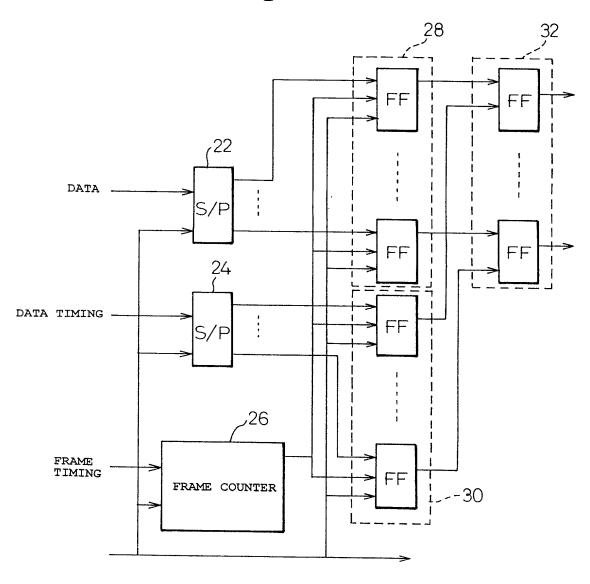
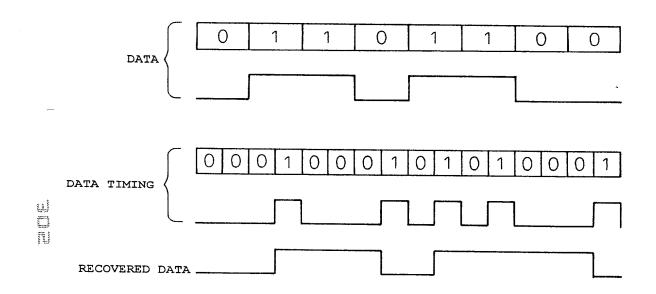
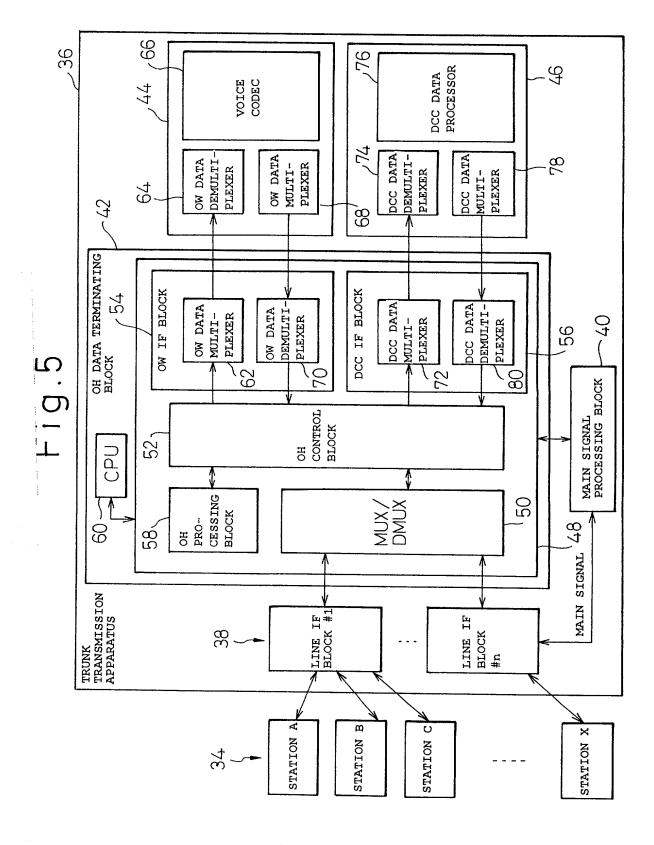
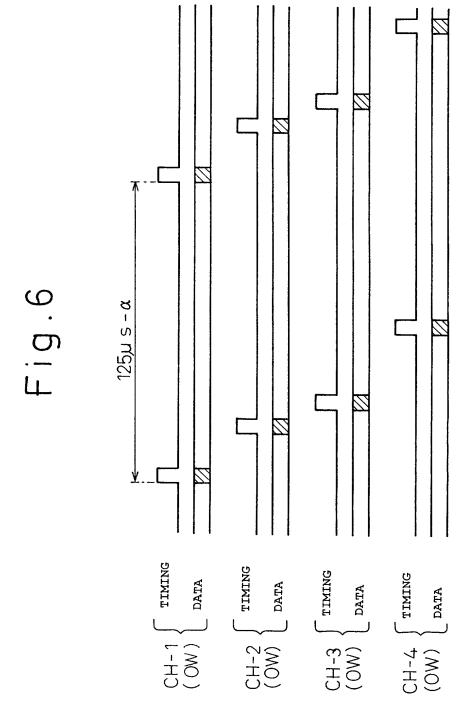


Fig.4



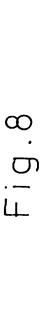


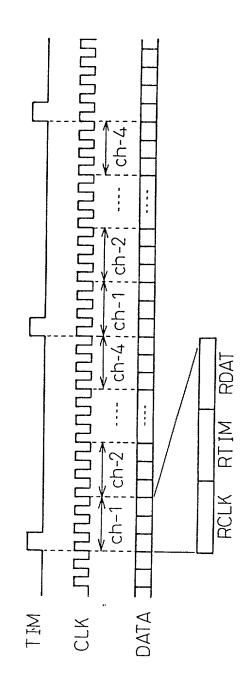
清楚的时候,我们就是一个时间,我们就是一个时间的时候,我们就是一个时间,我们是一个时间,我们也是一个时间,也是一个时间,我们也是一个时间,也是一个时间,也可以可



-64 77 89, OW DATA DEMULTI-PLEXER OW DATA MULTI-PLEXER OW UNIT TIM (135 KHZ CYCLE) TIM (135 KHZ CYCLE) CLK(1.62MHz) CLK(1.62MHz) Fig.7 DATA DATA 54 OW DATA MULTI-PLEXER OW DATA DEMULTI-PLEXER OW IF BLOCK 62 – 70-

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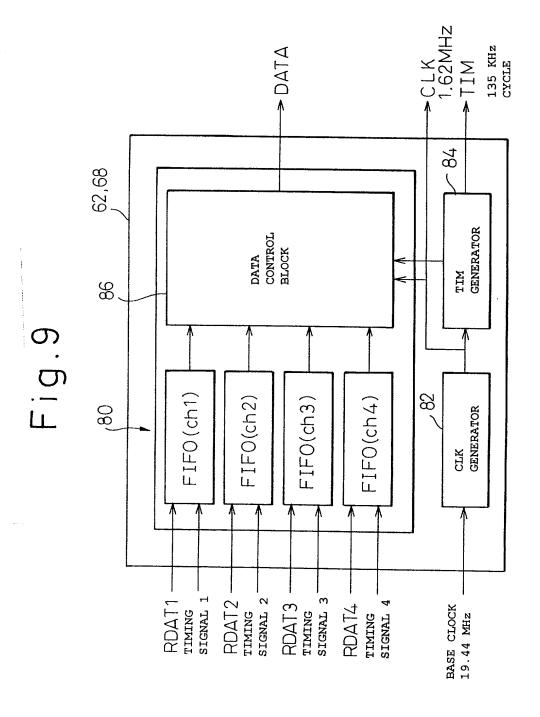
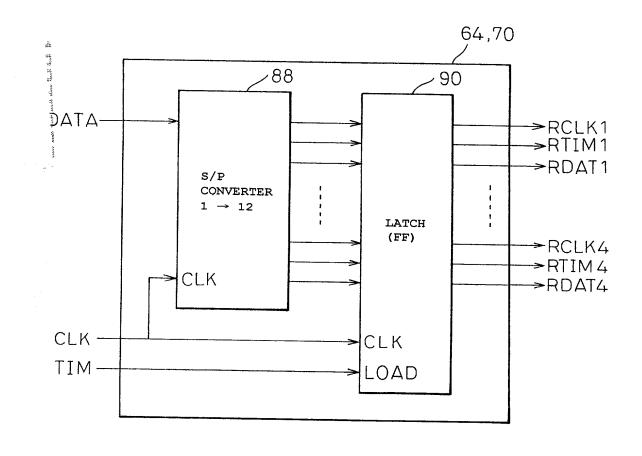


Fig.10

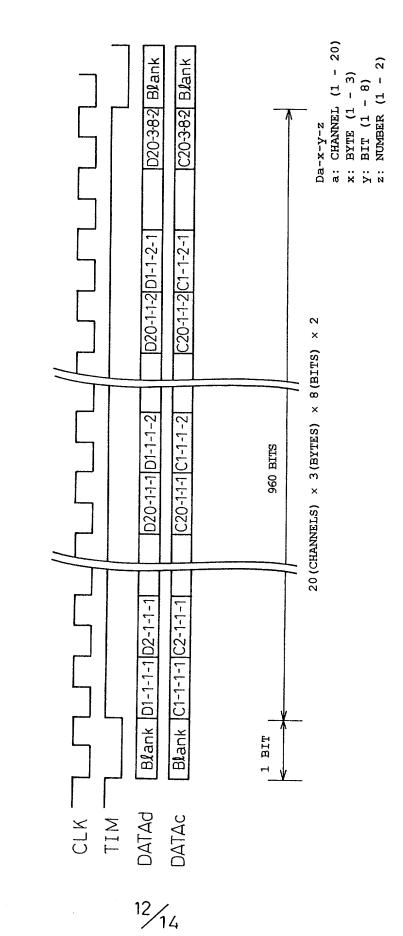


46 DCC DATA MULTIPLEXER DCC DATA DEMULTIPLEXER DCC UNIT TIM (10.11 KHZ CYCLE) TIM (10.11 KHZ CYCLE) Fig.11 CLK(9.72 MHz) CLK(9.72MHz) DATA_c DATA_c DATA_d DATA_d 56 DCC DATA MULTIPLEXER DCC DATA DEMULTIPLEXER DCC IF BLOCK 72 -80 7

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Fig.12



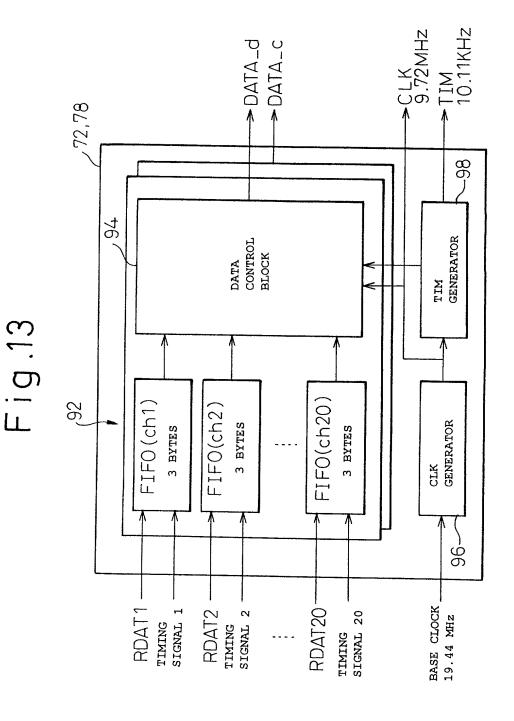


Fig.14

